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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,074	03/26/2001	Hachiro Fujita	204853US2	7350

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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,074	FUJITA ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8, 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/26/01, 1/23/02, 12/13/02, 1/8/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu et al. (A Parallel Decoding Scheme for Turbo Codes, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, ISCAS '98, 31 May- 3 June 1998, Volume: 4, Pages: 445 - 448).

Hsu et al. anticipate claim 1.

Hsu et al. teach a decoding unit for decoding a turbo-code sequence, said decoding unit comprising: a plurality of decoders for dividing a received code sequence into a plurality of blocks along a time axis, and for decoding at least two of the blocks in parallel, each decoder including a deinterleaver, an interleaver, and a decoding part (figure 2, 4a, 4b, 5, pages 445-447, Hsu et al.).

- Hsu et al. anticipate claim 2.

Hsu et al. teach the decoding unit further comprising a channel value memory for storing the received code sequence of the turbo-code and the received sequence of parity bit sequence of turbo-code (figure 5, pages 445-447, Hsu et al.).

- Hsu et al. anticipate claim 3.

Hsu et al. teach the decoding unit, wherein said plurality of decoders comprise at least a first decoder and a second decoder, each of which comprises a channel value memory interface including an interleave table for reading each of the plurality of blocks of a first and a second received code sequence from said channel value memory (figure 2, 5, pages 445, 447, Hsu et al.).

- Hsu et al. anticipate claim 4.

Hsu et al. teach the decoding unit, wherein each of said plurality of decoders comprises: a transition probability calculating circuit for calculating forward and reverse transition probabilities from channel values and prior values of each of the blocks; a path probability calculating circuit for calculating forward path probabilities from the forward transition probabilities, and reverse path probabilities from the reverse transition probabilities; a posterior value calculating circuit for calculating posterior values from the forward path probabilities, the reverse transition probabilities and the reverse path probabilities; and an external value calculating circuit for calculating external values for respective information bits by subtracting from the posterior values the channel values and the prior values corresponding to the information bits (figure 5, page 447, Hsu et al.).

- Hsu et al. anticipate claim 5.

Hsu et al. teach the decoding unit, wherein each of said plurality of decoders further comprises: means for supplying another of said decoders with one set of the forward path probabilities and the reverse path probabilities calculated finally; and an initial value setting circuit for setting the path probabilities supplied from another decoder as initial values of the path probabilities (figure 5, page 447, Hsu et al.).

- Hsu et al. anticipate claim 12.

Hsu et al. teach an encoding/decoding unit including an encoding unit for generating a turbo-code sequence from an information bit sequence and a decoding unit for decoding a turbo-code sequence (figure 1, 2, page 445, Hsu et al.), said encoding unit comprising: a first component encoder for generating a first parity bit sequence from the information bit sequence; an interleaver for interleaving the information bit sequence; a second component encoder for generating a second parity bit sequence from an interleaved information bit sequence output from said interleaver; and an output circuit for outputting the information bit sequence and the outputs of said first and second component encoders (figure 1, page 445, Hsu et al.), and said decoding unit comprising: a plurality of decoders each including a deinterleaver, an interleaver, and a decoding part, the plurality of decoders configured to divide a first received code sequence and a second received code sequence into a plurality of blocks along a time axis, and for decoding at least two

of the blocks in parallel, wherein the first received code sequence consists of a received sequence of the information bit sequence and a received sequence of the first parity bit sequence, and the second received code sequence consists of a bit sequence generated by interleaving the received sequence of the information bit sequence, and a received sequence of the second parity bit sequence; and the decoding unit further comprises a channel value memory for storing the first received code sequence and the received sequence of the second parity bit sequence (figures 2, 4a, 4b, 5, pages 445-447, Hsu et al.).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (A Parallel Decoding Scheme for Turbo Codes, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, ISCAS '98, 31 May- 3 June 1998, Volume: 4, Pages: 445 - 448) as applied to claim 2 above, and further in view of Yi (US 5,907,582).

As per claim 6, Hsu et al. substantially teach the claimed invention described in claim 2 (as rejected above).

However Hsu et al. do not explicitly teach the specific use of the decoding unit, wherein a first parity bit sequence of turbo-code and a second parity bit sequence of turbo-code are punctured

before transmitted, and wherein each of said decoders comprises a depuncturing circuit for inserting a value of least reliability in place of channel values corresponding to punctured bits of the received code sequences.

Yi in an analogous art teaches that in operation, the original audio program data sequences, represented as d.sub.k in FIG. 3, are supplied to the turbo encoder 122, which outputs an unaltered copy of the systematic audio data X.sub.1 to one input of MUX 142. The audio data d.sub.k is also supplied to the first constituent recursive encoder 134, which supplies parity output Y.sub.1, to one input of the first puncturer 138 and to one input of the second puncturer 140. The audio data d.sub.k are also supplied to interleaver 132. The second constituent encoder 136 is supplied with an interleaved audio program data signal d.sub.ki. Unaltered interleaved signal d.sub.ki is supplied in systematic form as sequence X.sub.2 to one input of MUX 144 for ultimate transmission to signal path 126. A copy of d.sub.ki is supplied to the second constituent encoder 136, which encodes each interleaved bit of audio data and generates a parity sequence Y.sub.2 which is supplied to both puncturers 138 and 140 (figure 3, col. 8, lines 51-67, Yi).

Yi also teaches that the code combiner 184 depunctures and achieves the code diversity combining so as to output systematic forms of uninterleaved audio signal sequence X.sub.1 and depunctured parity sequence Y.sub.1 to the first MAP decoder 186 which is symmetric to the first recursive systematic convolutional encoder 134 of the turbo encoder 122. The code combiner 184 also outputs systematic forms of interleaved audio signal sequence X.sub.2 and corresponding depunctured parity sequence Y.sub.2 to the packet code combiner 192 and depunctured parity sequence to the second MAP decoder 188 (figure 6, col. 12, lines 37-47, Yi).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hsu et al.'s patent with the teachings of Yi by including an additional step of using the decoding unit, wherein a first parity bit sequence of turbo-code and a second parity bit sequence of turbo-code are punctured before transmitted, and wherein each of said decoders comprises a depuncturing circuit for inserting a value of least reliability in place of channel values corresponding to punctured bits of the received code sequences.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that puncturing parity bits would provide the opportunity to increase the data transmission speed.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (A Parallel Decoding Scheme for Turbo Codes, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, ISCAS '98, 31 May- 3 June 1998, Volume: 4, Pages: 445 - 448) as applied to claim 4 above, and further in view of Wang (US 6,044,116).

As per claim 7, Hsu et al. substantially teach the claimed invention described in claim 4 (as rejected above).

However Hsu et al. do not explicitly teach the specific use of the decoding unit, wherein every time input of one of the blocks has been completed, each of said decoders starts decoding of the block, and outputs posterior values corresponding to the channel values of the block as posterior values corresponding to the information bits of the block.

Wang in an analogous art teaches that the turbo decoder includes first and second a-posteriori probability (APP) Decoders. The APP decoders compute a-posteriori probabilities of the digital bits. The output of the first APP decoder is a series of a-posteriori bias information, that is, a bias measurement of X based upon Y1. The X interleaved output, the first APP decoder interleaver output, and the Y2 input, all in interleaved order are fed into a second a-posteriori probability decoder providing the second APP decoder bias and bit estimate outputs in the interleaved order (col. 5, lines 50-51, lines 57-58, col. 6, lines 9-16, Wang).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hsu et al.'s patent with the teachings of Wang by including an additional step of using the decoding unit, wherein every time input of one of the blocks has been completed, each of said decoders starts decoding of the block, and outputs posterior values corresponding to the channel values of the block as posterior values corresponding to the information bits of the block.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to correct the errors by the APP decoder.

- As per claim 8, Hsu et al. and Wang teach the additional limitations.

Wang teaches the decoding unit, wherein at least one of said plurality of decoders decodes one of the blocks whose input has not yet been completed to generate posterior values of the block, and uses values corresponding to the posterior values as prior values of the block whose input has been completed (col. 5, lines 36-39, col. 12, lines 62-67, col. 13, lines 1-2, lines 17-23, Wang).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

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